19-2247; Rev 0; 10/01

MAXIM

Quad 2.5Gbps Cable Transceiver

General Description

The MAX3780 cable transceiver provides a bidirectional interface of four 2.5Gbps channels over low-cost copper cable or external fiber-optic interface. The transmitter section accepts eight channels of input at 1.25Gbps. An integrated 4-bit FIFO allows retiming of the transmit data to a clean local reference clock. The channels are multiplexed (2:1) into four outputs operating at 2.5Gbps. Pre-emphasis and equalization provide compensation for losses in low-cost cables up to 3m. The receiver recovers the clock and demultiplexes (1:2) the 2.5Gbps channels into eight 1.25Gbps outputs. Fully integrated phase-locked loops and delay-locked loops recover clock and data from the serial data inputs.

The transceiver IC is available in a compact 100-pin TQFP package with exposed-ground pad and consumes 2.2W.

Applications

Gigabit Ethernet Cable Backplane Concentration

System Interconnects Using Low-Cost Copper Cable

System Interconnects Using Parallel Optics

Features

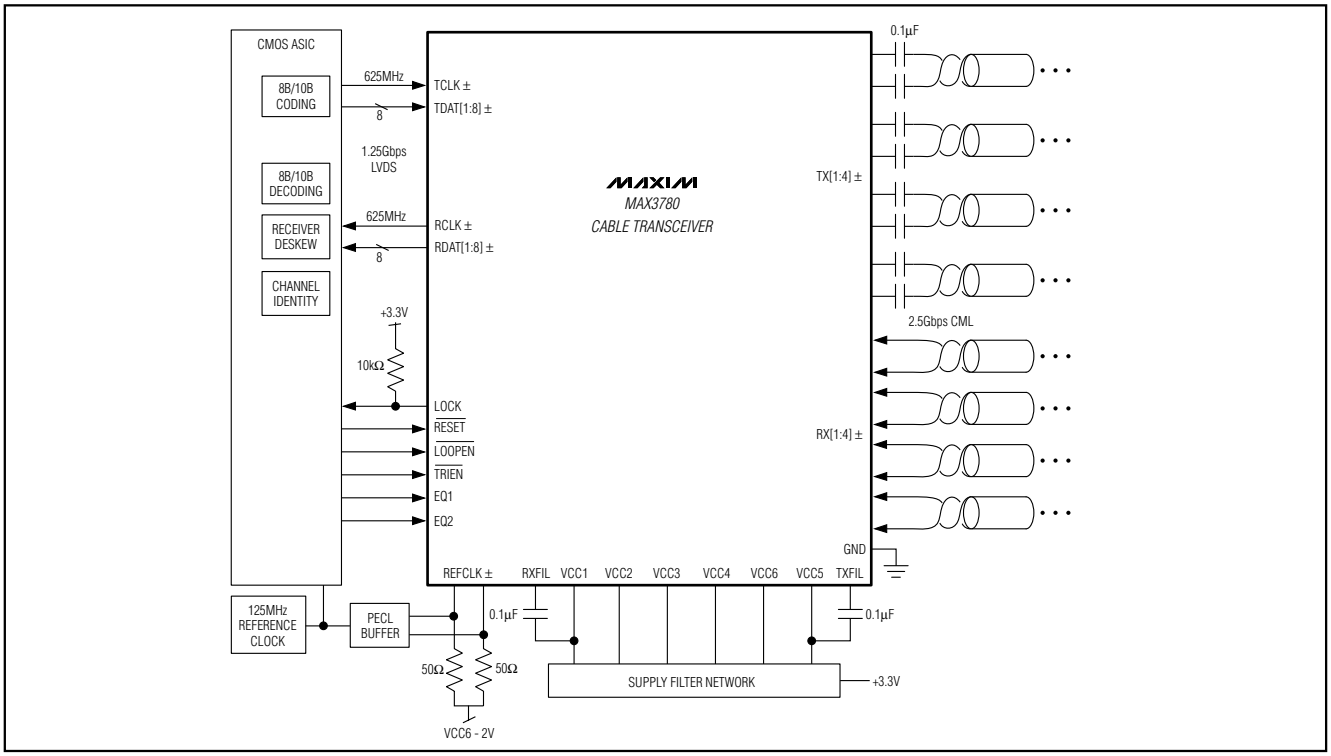
- ♦ **Quad 2:1 Channel Serialization**
- ♦ **Quad 1:2 Channel Deserialization**
- ♦ **3m Link Distance with Low-Cost Copper Cable**
- ♦ **Better than 10^{-16} BER Performance**
- ♦ **10Gbps Aggregate Parallel Interface**
- ♦ **System Loopback**
- ♦ **1.25Gbps LVDS Synchronous Interface**
- ♦ **2.5Gbps CML Serial Cable Interface**
- ♦ **PLL Lock Detect Signal**
- ♦ **Selectable Cable Pre-Emphasis**
- ♦ **Fixed Receive Equalization**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3780CCQ	0°C to +70°C	100 TQFP-EP*

**Exposed pad*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}1, V_{CC}2, V_{CC}3, V_{CC}4, V_{CC}5, V_{CC}6, VCCTEMP) .....-0.5V to +4.0V
Continuous CML Output Current .....-10mA to +25mA
Momentary CML Output Voltage (duration < 1 minute, +25°C).....0V to (V_{CC} + 0.5V)
CML Input Voltage.....-0.5V to (V_{CC} + 0.5V)
LVDS Input and Output Voltage.....-0.5V to (V_{CC} + 0.5V)
TTL Input or Output Voltage.....-0.5V to (V_{CC} + 0.5V)
PECL Input Voltage.....-0.5V to (V_{CC} + 0.5V)
TMPSENS, TXFIL, RXFIL Voltage.....-0.5V to (V_{CC} + 0.5V)
Operating Ambient Temperature Range .....0°C to +70°C
Operating Junction Temperature Range.....0°C to +150°C
Storage Ambient Temperature Range.....-55C° to +100°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Referenced to GND	3.0	3.3	3.6	V
Operating Ambient Temperature	T_A		0	25	70	°C
Power Dissipation			1.6	2.2	3.3	W
Supply Current	I_{CC}		533	665	916	mA
TTL INPUTS AND OUTPUTS						
TTL Input High Voltage	V_{IH}		2.0			V
TTL Input Low Voltage	V_{IL}				0.8	V
TTL Input High Current	I_{IH}	V_{IH} = 2.0V			-250	µA
TTL Input Low Current	I_{IL}	V_{IL} = 0V			-500	µA
TTL Output High Voltage	V_{OH}	Open collector, R_{LOAD} = 10kΩ	2.4			V
TTL Output Low Voltage	V_{OL}	R_{LOAD} = 10kΩ			0.4	V
PECL INPUTS						
PECL Input High Voltage		Referenced to V_{CC}6	-1165		-880	mV
PECL Input Low Voltage		Referenced to V_{CC}6	-1810		-1475	mV
PECL Input Current			-10		+10	µA
CML INPUTS (Note 1, Figure 5)						
Differential Input Voltage Range		Total differential signal required to achieve error rate	200		800	mVp-p
Single-Ended Input Voltage Range		Single-ended range of a differential input signal	V_{CC} - 0.5		V_{CC} + 0.2	V
Common-Mode Voltage		Inputs open or AC-coupled		V_{CC}		V
Input Impedance	R_{IN}	Differential	85	100	115	Ω
CML OUTPUTS (Note 1, Figure 4)						
Differential Output Voltage (Measured at the End of the Channel) (Note 3)		0m channel, EQ1 = 1, EQ2 = 1	400	600	800	mVp-p
		0.5m channel, EQ1 = 1, EQ2 = 1		540		
		1m channel, EQ1 = 1, EQ2 = 0		500		
		3m channel, EQ1 = 0, EQ2 = 1		400		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = 0°C to +70°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Common-Mode Voltage				V_{CC} - 0.3		V
Differential Output Impedance	R_{OUT}		85	100	115	Ω
LVDS INPUTS						
Input Voltage Range	V_I	$\|V_{GPD}\|$ < 925mV	0		2000	mV
Differential Input Voltage	$\|V_{ID}\|$	$\|V_{GPD}\|$ < 925mV	150		500	mV
Differential Input Impedance	R_{IN}		85	100	115	Ω
Input Common-Mode Current		V_{OS} = 1.2V, inputs tied together		-80	-200	µA
LVDS OUTPUTS (Note 2)						
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\|V_{OD}\|$		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	$\Delta\|V_{OD}\|$				25	mV
Output Offset Voltage	V_{OS}		1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\|V_{OS}\|$				25	mV
Differential Output Impedance	R_{OD}		80	100	120	Ω
Short-Circuit Current		Short to supply or ground			40	mA
Impedance When Disabled		$\overline{TRIEN}$ = 0	5	10		kΩ

Note 1: CML differential signal amplitudes are specified as the total signal across the load (V+ - V-).

Note 2: LVDS output signal amplitudes are specified according to IEEE 1596.3-1996.

Note 3: Differential output voltage is production tested for all EQ1 and EQ2 settings. Typical values are the differential peak-to-peak eye opening at the end of the cable.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = 0°C to +70°C, REFCLK = 125MHz, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER PARAMETERS						
TCLK Frequency				625		MHz
Transmitter Latency		From TDAT to TX		4.5		ns
LVDS INPUTS						
Accumulated Phase Error at TCLK		Relative to REFCLK		±0.8		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, LVDS differential load = 100Ω ±1%, CML differential load = 100Ω ±1%, T_A = 0°C to +70°C, REFCLK = 125MHz, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time	t_{SU}	Figure 1	100			ps
Hold Time	t_H	Figure 1	100			ps
CML OUTPUTS						
Deterministic Jitter		(Note 5)		15	25	ps_{p-p}
Random Jitter		Wideband jitter with 01 pattern (Note 7)		22	66	ps_{p-p}
Edge Speed	t_r, t_f	20% to 80%, measured at transmitter output, (EQ1 = 1, EQ2 = 1)			140	ps
RECEIVER PARAMETERS						
Clock Frequency				625		MHz
PLL Lock Time		After valid data applied		525		µs
Receiver Latency		From RX to RDAT		4.3		ns
Jitter Generation		(Note 7)		25	66	ps_{p-p}
LVDS OUTPUTS						
Clock Duty-Cycle Distortion	T_{PW}	Variation of 50% crossing from ideal time	-32		+32	ps
Deterministic Jitter		Measured with K28.5 pattern at RDAT_ outputs		15	50	ps_{p-p}
Edge Speed	t_r, t_f	20% to 80%		160	250	ps
Clock-to-Data Delay	τ_{CLK-Q}	Figure 2	268	400	532	ps
CML INPUTS						
High-Frequency Jitter Tolerance		(Note 6)	220	300		ps_{p-p}

Note 4: AC characteristics are guaranteed by design and characterization.
Note 5: Deterministic jitter (DJ) and differential output signal measured with K28.5 at TX_ pins.
Note 6: High-frequency jitter comprised of 164ps_{p-p} of deterministic jitter, 1.6ps_{RMS} random jitter, and the remaining as 5MHz sinusoidal jitter.
Note 7: Peak-to-peak random jitter is 16.4 × RMS jitter for a jitter probability of 10^{-16}.

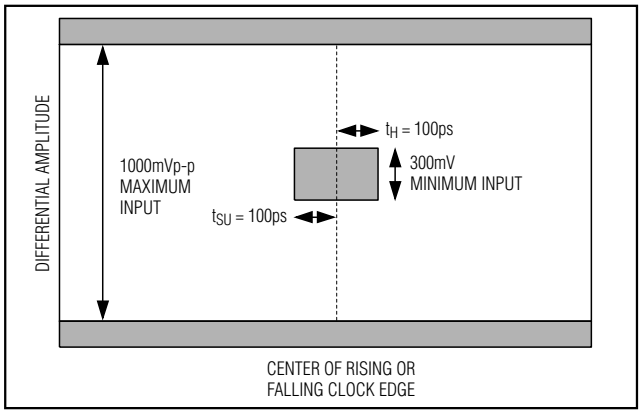


Figure 1. LVDS Receiver Input Eye Mask

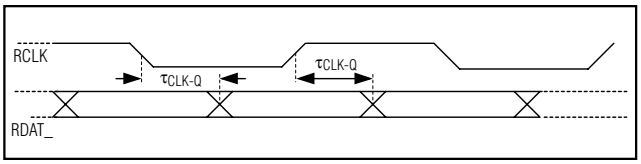
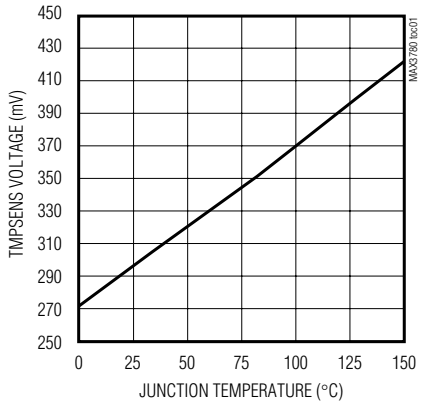


Figure 2. Definition of Clock-to-Q Delay

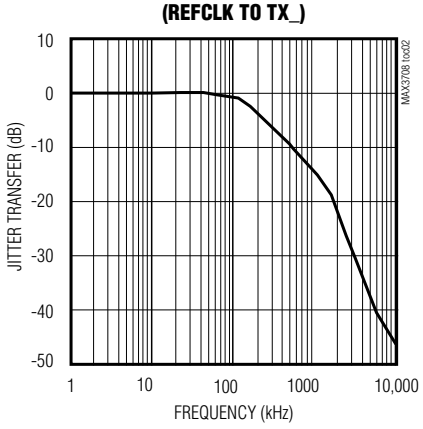
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

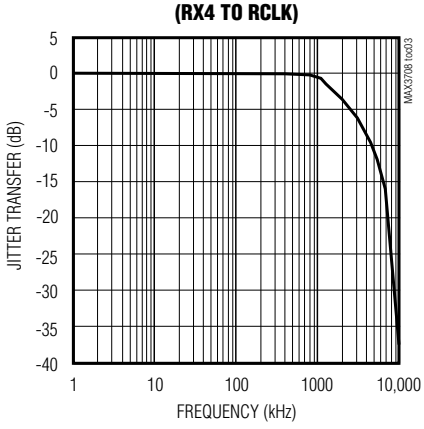
TMPSENS VOLTAGE vs. TEMPERATURE



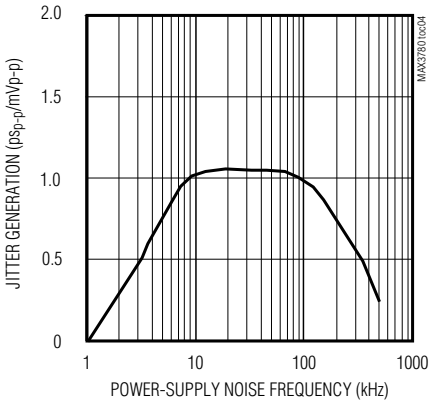
TRANSMITTER JITTER TRANSFER (REFCLK TO TX_)



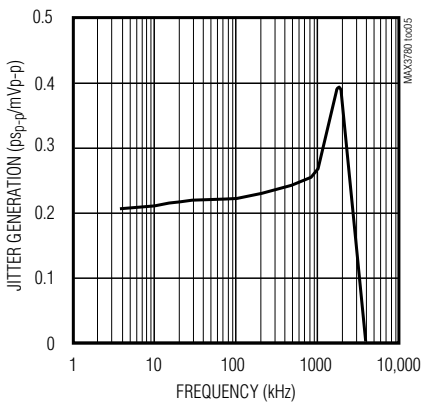
RECEIVER JITTER TRANSFER (RX4 TO RCLK)



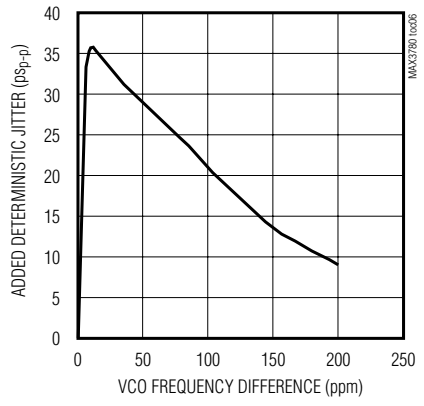
TRANSMITTER POWER-SUPPLY REJECTION



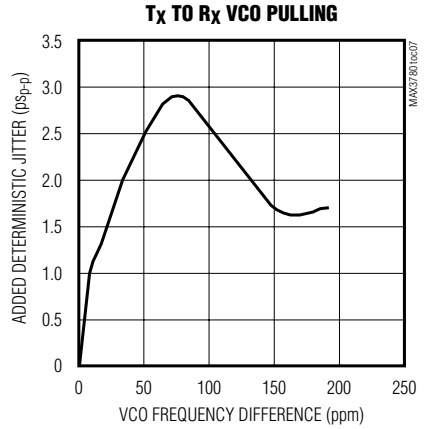
RECEIVER POWER-SUPPLY REJECTION



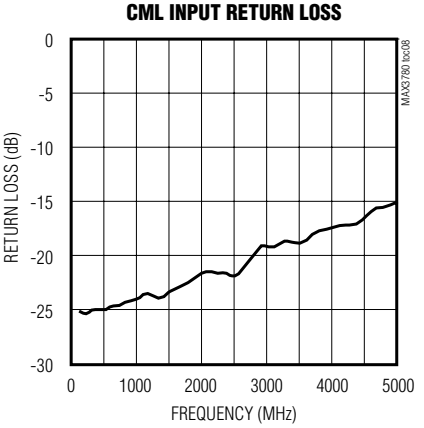
RX TO TX VCO PULLING



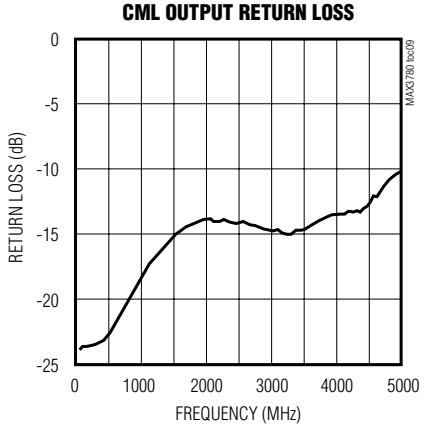
TX TO RX VCO PULLING



CML INPUT RETURN LOSS



CML OUTPUT RETURN LOSS

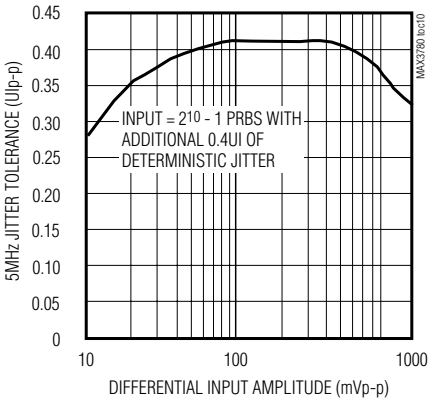


Quad 2.5Gbps Cable Transceiver

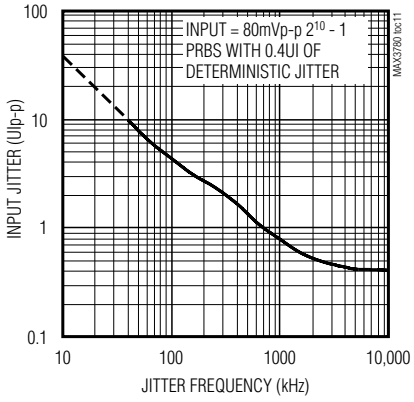
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

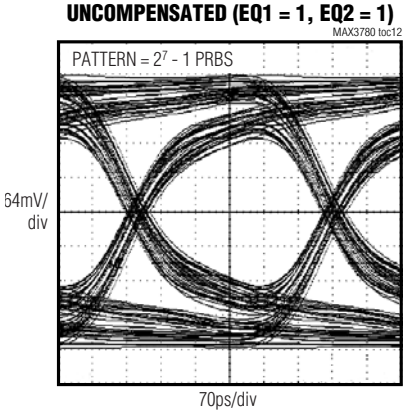
RX4 JITTER TOLERANCE vs. INPUT AMPLITUDE



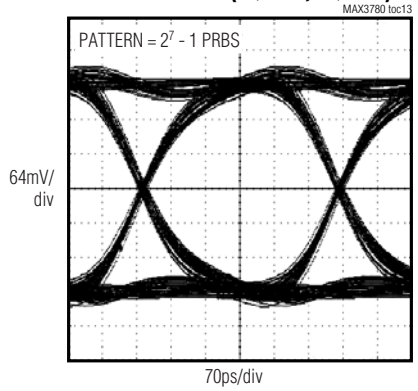
RX4 JITTER TOLERANCE



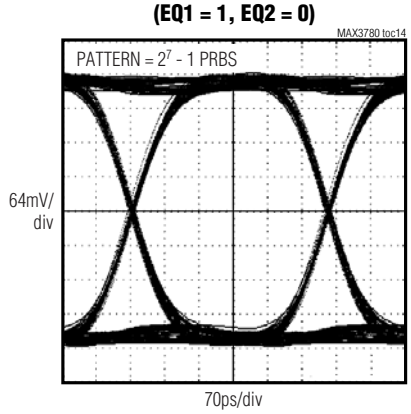
EYE DIAGRAM AFTER 3m CABLE UNCOMPENSATED (EQ1 = 1, EQ2 = 1)



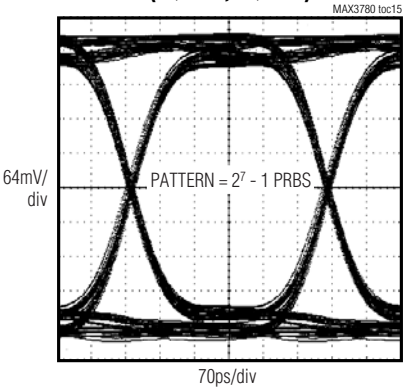
EYE DIAGRAM AFTER 3m CABLE COMPENSATED (EQ1 = 0, EQ2 = 1)



EYE DIAGRAM AFTER 1.0m CABLE (EQ1 = 1, EQ2 = 0)



EYE DIAGRAM AFTER 0.5m CABLE (EQ1 = 1, EQ2 = 1)



Pin Description

PIN	NAME	FUNCTION
1, 12, 25, 26, 28, 31, 45, 50, 51, 55, 63, 71, 75, 76, 80, 100	GND	Supply Ground
2, 11, 24	VCC1	+3.3V Supply for Receiver, LVDS Data and Clock Outputs, and Digital Receiver Functions
3, 5, 7, 9, 13, 15, 17, 19	RDAT1+ to RDAT8+	Positive Parallel-Data Outputs, LVDS
4, 6, 8, 10, 14, 16, 18, 20	RDAT1- to RDAT8-	Negative Parallel-Data Outputs, LVDS
21	RCLK+	Positive 625MHz Recovered Clock, LVDS. Parallel-data outputs are clocked on both the rising and falling edge of the clock.
22	RCLK-	Negative 625MHz Recovered Clock, LVDS. Parallel-data outputs are clocked on both the rising and falling edge of the clock.
23	$\overline{\text{TRIEN}}$	Three-State Enable, TTL Input. Setting $\overline{\text{TRIEN}}$ low forces the LVDS outputs into a high-impedance state and the LOCK pin to a logical '1'. CML outputs are not affected by $\overline{\text{TRIEN}}$. Internally pulled high through 15kΩ.
27	LOCK	Lock Status Indicator, TTL Output. This output goes high when the transmit PLL, receiver PLL, and receiver DLLs are in lock. Because this output is open-collector TTL, it requires an external 10kΩ pullup resistor to V_{CC}. The LOCK pins from multiple MAX3780s can be connected in parallel to form a single LOCK signal.
29	RXFIL	Receiver Loop Filter Connection. Connect a 0.1µF capacitor between RXFIL and VCC2.
30	VCC2	+3.3V Supply for Receiver VCO, Analog Receiver Functions, and External Loop Filter Connection
32, 35, 38, 41, 44	VCC3	+3.3V Supply for CML Inputs
33, 36, 39, 42	RX4- to RX1-	Negative Serial Input, CML
34, 37, 40, 43	RX4+ to RX1+	Positive Serial Input, CML
46, 79, 99	VCC6	+3.3V Supply for LVDS Inputs, FIFO, Multiplexer, and PECL REFCLK Input
47	$\overline{\text{LOOPEN}}$	Loopback Enable, TTL input. Force low to enable system loopback. Internally pulled high through 15kΩ.
48	VCCTEMP	+3.3V Supply for TMPSENS. Connect to ground to disable the temperature-sensing circuit.
49	TMPSENS	Junction Temperature Sensor. Analog output corresponding to the junction temperature of the die. Leave open for normal use.
52	PTPIN	Reserved for Maxim Use. Connect to ground for normal operation.
53	EQ2	Transmit Equalizer Control Input #2, TTL. Refer to Table 1 for setting transmitter precompensation. Internally pulled high.
54	EQ1	Transmit Equalizer Control Input #1, TTL. Refer to Table 1 for setting transmitter precompensation. Internally pulled high.
56, 59, 62, 64, 67, 70	VCC4	+3.3V Supply for CML Outputs

Quad 2.5Gbps Cable Transceiver

Pin Description (continued)

PIN	NAME	FUNCTION
57, 60, 65, 68	TX4- to TX1-	Negative Serial Output, CML
58, 61, 66, 69	TX4+ to TX1+	Positive Serial Output, CML
72	$\overline{\text{RESET}}$	Reset Input, TTL. Connect low for >80ns to reset FIFO and receiver components. Internally pulled high through 15kΩ.
73	TXFIL	Transmitter Loop Filter Connection. Connect a 0.1µF capacitor between TXFIL and VCC5.
74	VCC5	+3.3V Supply for Transmitter VCO, Analog Transmitter Functions, and External Loop Filter Connection
77	REFCLK+	Positive Reference Clock Input, PECL
78	REFCLK-	Negative Reference Clock Input, PECL
81	TCLK+	Positive Clock Input for Transmitter Input Data, LVDS
82	TCLK-	Negative Clock Input for Transmitter Input Data, LVDS
83, 85, 87, 89, 91, 93, 95, 97	TDAT1+ to TDAT8+	Positive Parallel Data Inputs, LVDS
84, 86, 88, 90, 92, 94, 96, 98	TDAT1- to TDAT8-	Negative Parallel Data Inputs, LVDS

Detailed Description

The MAX3780 cable transceiver uses four 2:1 muxes and four 1:2 demuxes to simplify backplane routing. The serial transceiver interface can either be a fiber module or up to 3m of low-cost, twisted-pair copper cable. This bidirectional interface provides low-voltage differential signaling (LVDS) interfaces at the 1.25Gbps parallel inputs and outputs. The serial data inputs and outputs utilize current-mode logic (CML) structures. An integrated PLL recovers the clock from the incoming serial data, as well as retimes the received data.

The serial interface uses both precompensation as well as equalization to allow high-speed transmission through up to 3m of copper cable while maintaining a BER < 10^{-16}. The compensation/equalization circuits are optimized for short cables, 0.5m cables, 1m cables, or 3m cables. TTL inputs are provided to select the amount of precompensation.

LVDS Inputs and Outputs

The MAX3780 parallel interface includes eight differential data inputs at 1.25Gbps, one half-rate differential clock input at 625MHz, eight differential data outputs at 1.25Gbps, and one half-rate differential clock output at 625MHz. All parallel inputs and outputs are LVDS compatible to minimize power dissipation, speed transition time, and improve noise immunity. The LVDS outputs go into a high-impedance state when $\overline{\text{TRIEN}}$ is forced low. This simplifies system checks by allowing vectors to be forced on the LVDS outputs. The LVDS outputs also have short-circuit protection in case of shorts to VCC or GND.

PLL Clock Multiplier

The PLL clock multiplier uses the 125MHz reference clock to synthesize 1.25GHz and 2.5GHz clocks used to synchronize the transmitter functions. The reference clock is also used to aid frequency acquisition in the receiver. The 125MHz input signal at REFCLK requires a duty cycle between 40% and 60%. To achieve proper jitter performance and BER benchmarks, it is critical to use a high-quality, low-jitter reference clock. See the *Reference Clock Requirements* table for more information.

Bit-Interleaved Multiplexer/Demultiplexer

The MAX3780 uses bit interleaving to multiplex the parallel data and bit deinterleaving to demultiplex the serial data. After serial transmission, the channel assignment of the parallel outputs is random for each serial channel. In other words, there is a 50% chance that RDAT1 = TDAT1 and RDAT2 = TDAT2 and a 50% chance that RDAT1 = TDAT2 and RDAT2 = TDAT1. Because the MAX3780 does not perform channel assignment, other circuitry must handle this task.

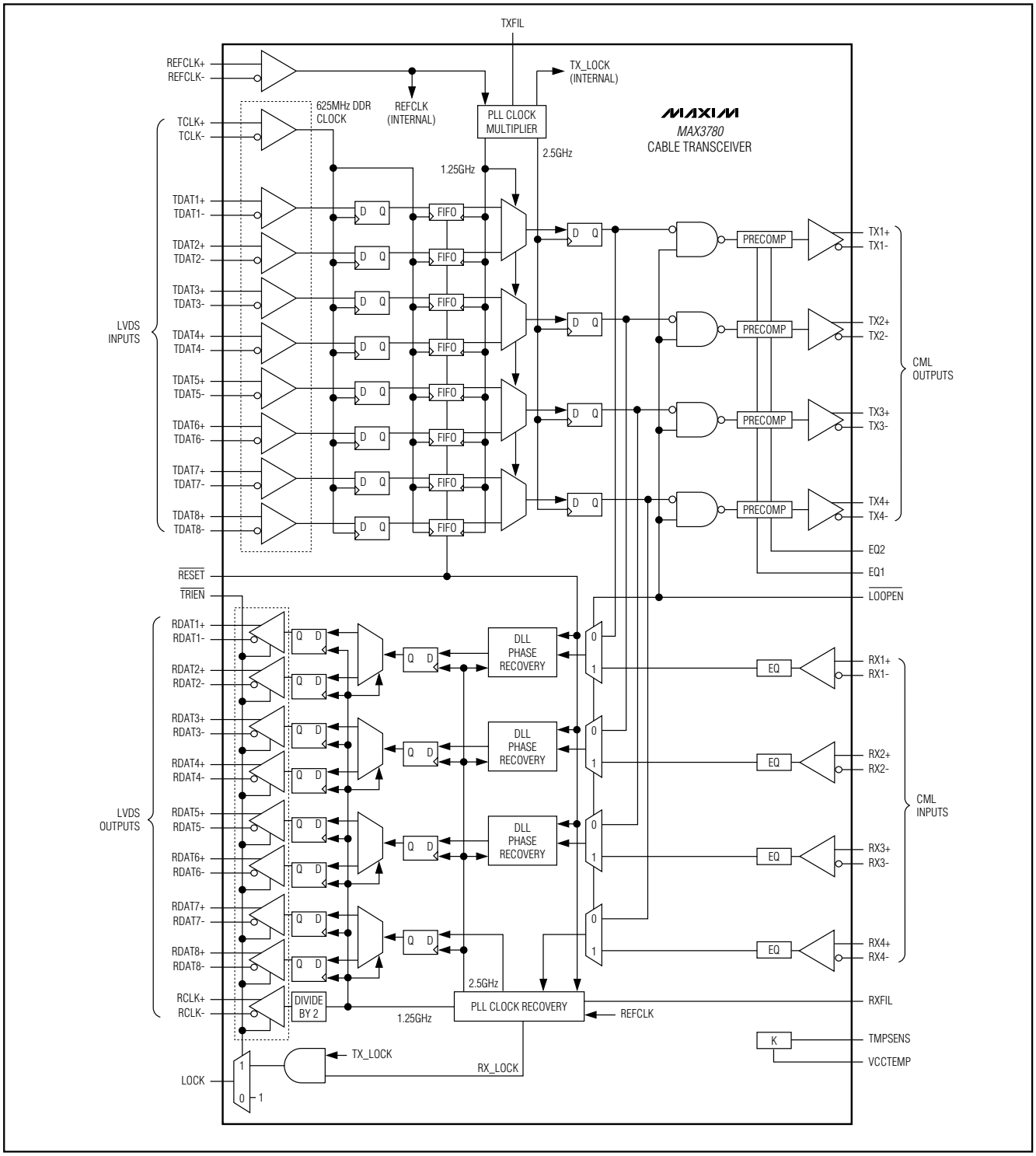


Figure 3. Functional Diagram

Table 1. Setting the CML Output Precompensation

RECOMMENDED CHANNEL	PRECOMPENSATION VALUE	EQ1	EQ2
Extended Range	30%	0	0
3m Cable	20%	0	1
1m Cable	10%	1	0
0.5m Cable or Fiber Module	Off	1	1

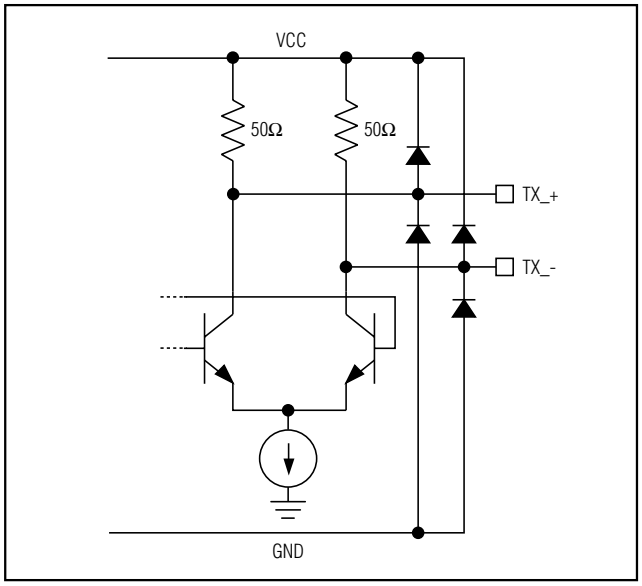


Figure 4. Simplified CML Output Structure

PLL Clock Recovery

The phase-locked loop recovers a synchronous clock signal from the incoming serial data on RX4. This recovered clock is then used to retime all four channels of incoming serial data before demultiplexing. Phase alignment on channels RX1, RX2, and RX3 is achieved by using delay-locked loops. The typical loop bandwidth of the PLL clock recovery circuit is 1.5MHz.

Delay-Locked Loop (DLL) Phase Recovery

The delay-locked loops in the RX1, RX2, and RX3 receive path are used to phase align the incoming data to the clock generated by the PLL. Because all serial channels originate from the same source and travel down the same cable, it is assumed that the low-frequency jitter on channel 4 is common to all channels. This allows the PLL to maintain frequency/phase alignment, and the DLLs only serve as adjustable delay lines to allow for different channels to have different (static) phase relationships.

CML Outputs with Precompensation

The serial outputs of the MAX3780 (TX1–TX4) are CML compatible. These outputs offer the best combination of low power dissipation, performance, and external component count. AC-coupling capacitors should always be used to provide immunity to common-mode voltage mismatches. The CML output structure is shown in Figure 4. For more information, refer to the applications note HFAN 01.0 *Introduction to LVDS, PECL, and CML*. Table 1 gives the amount of compensation for different EQ1 and EQ2 settings.

The CML data outputs have adjustable precompensation to compensate for cable and PC board trace losses. The cable and PC board traces have skin-effect and dielectric losses that attenuate high frequencies more than low frequencies. The precompensation FIR filter does the inverse. It attenuates low frequencies and boosts high frequencies. If precompensation is chosen to match the channel attenuation, the data at the end of the cable will be equalized.

CML Inputs with Equalization

The CML input structure, shown in Figure 5, provides low power dissipation and excellent performance. The CML inputs have integrated 50Ω termination resistors, reducing the external component count required for interfacing.

The CML inputs of the MAX3780 (RX1–RX4) provide equalization to further compensate for cable losses. The equalization circuit will typically add about 2dB of boost at 2GHz.

Lock Detection

The LOCK output indicates the state of both the transmitter and receiver PLLs. For lock detect to be asserted high, both the transmitter and receiver internal-lock indicators must be high for 394µs. The internal lock signals go high once frequency lock has been achieved. For LOCK to be asserted low, either the transmitter or receiver internal-lock indicators must be low for a minimum of 1053µs. LOCK is also asserted low when $\overline{\text{RESET}}$ is forced low. LOCK will stay low for a minimum of 394µs. For the lock detector to function properly, there must be data transitions at the RX4 input and a valid reference clock input. **Note:** The LOCK output is not an accurate indicator of signal presence at the receiver inputs. With no data input, the LOCK output can be high, low, or toggling.

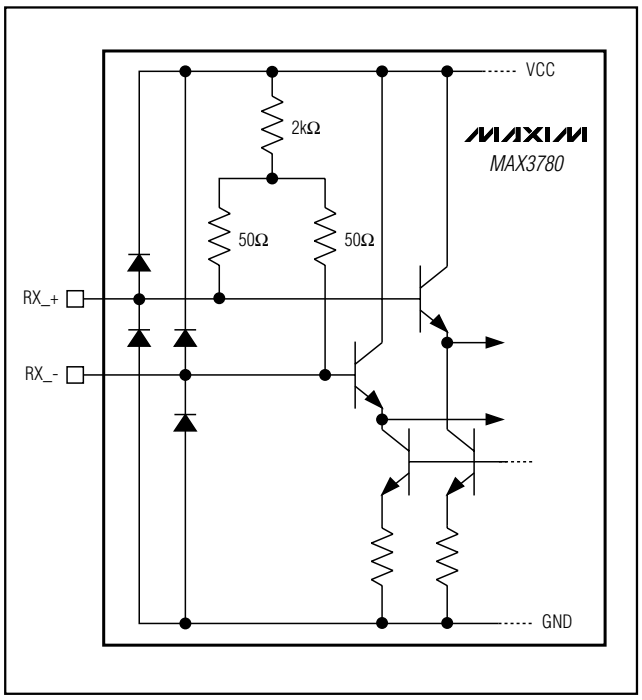


Figure 5. CML Input Structure

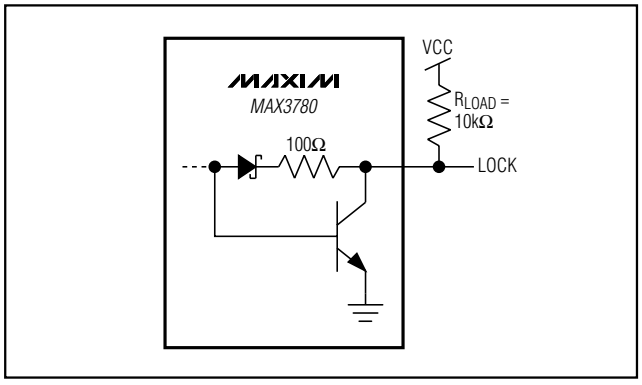


Figure 6. LOCK Output Structure

$\overline{\text{RESET}}$ Input

Approximately 10ms or longer after power-up, the $\overline{\text{RESET}}$ input should be asserted low. $\overline{\text{RESET}}$ must be held low for a minimum of four reference clock cycles for it to be properly asserted. $\overline{\text{RESET}}$ is used to reset the lock state, FIFO clock logic, and delay-lock loops.

Temperature Sensor

To aid in evaluation of thermal performance, a temperature sensor is incorporated into the MAX3780. The temperature sensor may be powered on or off regardless of the state of the rest of the chip. The VCCTEMP pin provides supply voltage for the temperature sensor circuit. The TMPSENS output is designed to output a voltage proportional to the die junction temperature (1mV per Kelvin). The temperature of the die can be estimated as:

$$T(^{\circ}C) \approx V_{TEMPSENS}(mV) \times \frac{1^{\circ}C}{mV} - 273^{\circ}C$$

Applications Information

BER Calculation

Digital transmission systems will always, given enough time, have errors. This is due to the random nature of both voltage noise and timing noise, or jitter. In today's high performance digital transmission systems, we often try to measure bit error ratios (BERs) of fewer than 1 error every 10,000,000,000 bits ($BER < 10^{-10}$). Measuring such low error rates can prove to be problematic, since even at high data rates, the testing time required to obtain statistically significant results becomes impractical. (For more information, refer to HFTA-05.0 *Statistical Confidence Levels for Calculating Error Probability*.)

The MAX3780 serial interface operates at 2.5Gbps and is designed to operate with a BER better than 10^{-16} (1 error every 10,000,000,000,000,000 bits). This will give, on average, one error every 46 days on each 2.5Gbps channel. It is practically impossible to directly test such a low BER. For this reason, we turn to mathematics to ensure that this incredible BER is met.

The thermal noise in the MAX3780 serial channel is low ($<1mV_{RMS}$ in the CML receiver). The dominant voltage noise in the serial channel is due to crosstalk. The remaining impairments are various types of timing jitter due to clock nonidealities and data-dependant jitter. In this section, all calculations will be done in the time domain (similar to the draft technical report by ANSI T11.2, Project 1230, *Fibre Channel—Methodologies for Jitter Specification*) where timing jitter is applied directly and voltage noise is converted into an equivalent timing jitter. The equation relating timing jitter to error rate is below:

$$1UI = \Sigma DJ_{p-p} + \alpha \times \sqrt{\Sigma RJ^2_{RMS}}$$

Table 2. Summary of Jitter Parameters Contributing to the BER Calculation

PARAMETER		DETERMINISTIC COMPONENTS		RANDOM COMPONENTS	
		TYPICAL (mUIp-p)	WORST-CASE (mUIp-p)	TYPICAL (mUI_{RMS})	WORST-CASE (mUI_{RMS})
Reference Clock—Random				0.19	0.38
Reference Clock—Deterministic		5	10		
Transmitter—Random				3.25	10
Transmitter—Oscillator Pulling		8.75	23.75		
Transmitter—Supply Noise		2.5	7.5		
Transmitter—Output Stage		37.5	62.5		
Channel—Cable Losses		50	112.5		
Channel—Crosstalk		28	56		
Channel—Mismatched Load		12.5	25		
Receiver—VCO Phase Noise				3.75	10
Receiver—Input-Referred Noise				1.25	2.5
Receiver—Sampling Offset		187.5	387.5		
Receiver—Oscillator Pulling		7.5	15		
Receiver—Supply Noise		6.25	18.75		
TOTALS =		345.5	718.5	5.12	14.37
		TYPICAL	**WORST-CASE**		
	ALPHA =	**127.8**	**19.6**		
	BER =	**~0**	**5.7×10^{-23}**		

Deterministic jitter and receiver sampling offset effectively reduce the amount of time that the receiver can sample without error. Errors occur at a rate determined by α:

$$\alpha = \frac{1 - \Sigma DJ_{p-p}}{\sqrt{\Sigma RJ^2_{RMS}}}$$

An α >16.4 corresponds to a BER < 10^{-16}. Refer to Maxim applications note HFAN-4.0.2 *Converting Between RMS and Peak-to-Peak Jitter at a Specified BER.*

For a discussion of deterministic jitter and random jitter and the characteristics of each, refer to Maxim applications note HFAN-4.0.3 *Jitter in Digital Communication Systems, Part 1.*

Table 2 shows the deterministic and random components used in the BER calculation for the MAX3780. Typical and worst-case numbers are presented. The worst-case estimate represents a BER with greater than 6-sigma margin. Many of the worst-case components are uncorrelated variables that are taken to their individual 6-sigma limits.

In summary, the predicted worst-case BER = 10^{-20}. A typical channel will operate error free.

All transmitter and channel jitter components are compared to the jitter tolerance of the receiver by translating the components to equivalent phase error in the receiver. Low-frequency jitter components are tracked by the receive PLL, and therefore contribute little to the phase error. High-frequency jitter components (beyond the loop bandwidth of the receiver) are not tracked by the receiver PLL and therefore directly translate to phase error. The phase error transfer function is essentially equivalent to the inverse of the jitter tolerance versus frequency with the high-frequency portion normalized to unity.

Reference Clock—Random

A maximum random jitter of 15ps$_{RMS}$ for frequencies less than 5kHz is stated as a requirement for the reference clock in the *Reference Clock Requirements* section. Translating this to the phase error of the receiver gives 75fs$_{RMS}$ (0.19mUI$_{RMS}$) typical and 150fs$_{RMS}$ (0.38mUI$_{RMS}$) worst-case.

Reference Clock—Deterministic

A maximum deterministic jitter of 20ps$_{p-p}$ for frequencies greater than 5kHz is stated as a requirement for the reference clock in the *Reference Clock Requirements* section. Combining the low-pass jitter transfer of the transmitter and the high-pass phase error transfer of the receiver results in a bandpass transfer function. For design margin, it is assumed that this deterministic jitter is within the bandpass frequency range. The typical deterministic component is 2ps$_{p-p}$ (5mUIp-p) and the worst-case entry is 4ps$_{p-p}$ (10mUIp-p).

Transmitter—Random

This is the random jitter that results from the transmitter VCO phase noise and is an AC parameter guaranteed in the *AC Electrical Characteristics* table. Typical measured numbers are 1.3ps$_{RMS}$ (3.3mUI$_{RMS}$) and the worst-case specification is 4.0ps$_{RMS}$ (10mUI$_{RMS}$).

Transmitter—Deterministic

1) Oscillator Pulling

The transmitter and receiver integrated LC oscillators when running at small frequency differences will beat with each other at a rate equivalent to the frequency difference between the oscillators. *Typical Operating Characteristic* plot RX to TX VCO PULLING shows the typical transmitter jitter versus frequency difference. When referred to the phase error transfer, the deterministic jitter is typically 3.5ps$_{p-p}$ (8.75mUIp-p) and 9.5ps$_{p-p}$ (23.75mUIp-p) worst-case.

2) Supply Noise

Noise on the power supply will modulate the transmit PLL output according to the typical transfer curve shown in the *Typical Operating Characteristic* plot TRANSMITTER POWER-SUPPLY REJECTION. Combining this transfer function with the phase error transfer of the receiver results in a band-pass characteristic. At the peak of this band pass, the typical transfer is 100fs/mV and the worst-case transfer is 300fs/mV. Making the worst-case assumption that all the supply noise is at this peak with a value of 10mV results in typically 1ps$_{p-p}$ (2.5mUIp-p) and worst-case 3ps$_{p-p}$ (7.5mUIp-p).

3) Output Stage

Finite bandwidth and pulse-width distortion in the serial transmitter can cause deterministic jitter in the serial data stream. Characterization and simulation results tell us the deterministic jitter is typically 15ps$_{p-p}$ (37.5mUIp-p) and 25ps$_{p-p}$ (62.5mUIp-p) worst-case.

Channel—Deterministic

1) Cable Losses

The frequency-dependent skin-effect and dielectric losses in the cable (and PC board traces) will cause data-dependent jitter (also known as intersymbol interference). Adjustable transmit precompensation and fixed receiver boost is used to reduce the cable-induced jitter. However, there will always be some uncompensated jitter due to the cable and PC board trace losses. Characterization and simulation results tell us the deterministic jitter is typically 20ps$_{p-p}$ (50mUIp-p) and 45ps$_{p-p}$ (112.5mUIp-p) worst-case.

2) Crosstalk

The MAX3780 channel requirements allow for crosstalk of up to 5% to be present at the RX inputs. This is a peak-to-peak voltage measurement which refers to 5% of the transmitter amplitude. Characterization and simulation results tell us the deterministic jitter due to crosstalk is typically 11.2ps$_{p-p}$ (28mUIp-p) and 22.4ps$_{p-p}$ (56mUIp-p) worst-case.

3) Mismatched Load Jitter

Incorrect impedances in PC board traces, connectors, cables, and terminations can cause reflections that can, in turn, cause deterministic jitter. These effects are more pronounced on short cables (less attenuation of the reflection) where timing margins are highest. While measurements already account for mistermination effects, we have allocated an additional fixed budget for jitter induced by reflections. Characterization and simulation results tell us the deterministic jitter due to load mismatch is typically 5ps$_{p-p}$ (12.5mUIp-p) and 10ps$_{p-p}$ (25mUIp-p) worst-case.

Receiver—Random

1) VCO Phase Noise

This is the random jitter that results from the receiver VCO phase noise and is an AC parameter guaranteed in the *AC Electrical Characteristics* table. Typical measured numbers are 1.5ps$_{RMS}$ (3.75mUI$_{RMS}$) and the worst-case specification is 4ps$_{RMS}$ (10mUI$_{RMS}$).

2) Input-Referred Noise

All electronic circuits generate random noise. The input-referred noise voltage of the CML RX inputs is < 0.5mV$_{RMS}$. This will contribute <1ps$_{RMS}$ jitter. In the BER calculation, it is assumed the jitter is typically 0.5ps$_{RMS}$ (1.25mUI$_{RMS}$) and 1ps$_{RMS}$ (2.5mUI$_{RMS}$) worst-case.

Receiver—Deterministic

1) Sampling Offset

The peak-to-peak sampling offset in the receiver is equal to 1UI minus the jitter tolerance minus the random jitter of the receiver. Removal of the random jitter is necessary since receiver VCO Phase Noise in Table 2 accounts for this. For simplicity, the random jitter portion will be assumed to be the typical measured value of 25ps$_{p-p}$ (62.5mUIp-p). Using the numbers from the AC parameter electrical table, the typical sampling offset is calculated to be 187.5mUIp-p and the worst-case is 387.5mUIp-p.

2) Oscillator Pulling

The transmitter and receiver integrated LC oscillators, when running at small frequency differences, will beat with each other at a rate equivalent to the frequency difference between the oscillators. *Typical Operating Characteristic* plot TX to RX VCO PULLING shows the typical receiver jitter versus frequency difference. Typically the receiver oscillator pulling jitter is 3ps$_{p-p}$ (7.5mUIp-p) and worst-case is 6ps$_{p-p}$ (15.0mUIp-p).

3) Supply Noise

Noise on the power supply will modulate the receive PLL sampling point according to the typical transfer curve shown in *Typical Operating Characteristic* plot RECEIVER POWER-SUPPLY REJECTION. Using a typical transfer of 250fs/mV and a worst-case transfer of 750fs/mV with 10mV of supply noise results in 2.5ps$_{p-p}$ (6.25mUIp-p) and 7.5ps$_{p-p}$ (18.75mUIp-p) respectively.

Low-Voltage Differential Signal (LVDS) Inputs/Outputs

The MAX3780 has LVDS inputs and outputs for interfacing with high-speed digital circuitry. All LVDS inputs and outputs are compatible with the IEEE-1596.3 LVDS specification. This technology uses 250mV to 400mV differential low-voltage amplitudes to achieve fast transition times, minimize power dissipation, and improve noise immunity. For proper operation, the parallel clock and data LVDS outputs (RCLK+, RCLK-, RDAT_+, RDAT_-) require 100Ω differential DC terminations between the inverting and noninverting outputs. Do not terminate these outputs to ground. The parallel data LVDS inputs (TCLK+, TCLK-, TDAT_+, TDAT_-) are internally terminated with 100Ω differential input resistance and therefore do not require external termination.

The LVDS inputs must be biased for proper operation. DC-coupling LVDS outputs and inputs together provides sufficient biasing. When interfacing to laboratory test equipment, AC-coupling cannot be used. A signal source with DC offset must be used.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies, keep ground connections short, and use multiple vias where possible. Use controlled-impedance 50Ω transmission lines to interface with the MAX3780 high-speed inputs and outputs.

Place power-supply decoupling as close to V_{CC} as possible. To reduce feedthrough, take care to isolate the input signals from the output signals.

Exposed-Pad (EP) Package

The exposed-pad 100-pin TQFP-EP incorporates features that provide a very low thermal resistance path for heat removal from the IC. The pad is electrical ground on the MAX3780 and must be soldered to the circuit board for proper thermal and electrical performance.

Channel Requirements

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Impedance		Differential		100		Ω
Through Loss at 1GHz	(S12, S21)	f = 1GHz, 3m channel	4.0	5.0	6.0	dB
		f = 1GHz, 1m channel	1.5	2.4	3.2	
		f = 1GHz, 0.5m channel	1.0	1.7	2.6	
Wideband Through Loss	(S12, S21)		See Figures 7–9			
Return Loss at 1GHz	(S11, S22)				-12	dB
Wideband Return Loss	(S11, S22)		See Figure 10			
Channel Crosstalk		% of signal at aggressor. Near-end and far-end aggressors driven with 100ps (20% to 80%) edges. End of channel terminated with 100Ω.			5	%

Reference Clock Requirements

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFCLK Frequency				125		MHz
REFCLK Frequency Tolerance			-100		+100	ppm
REFCLK Duty Cycle			40		60	%
REFCLK Jitter		f < 5kHz (jitter assumed Gaussian)			240	ps_{p-p}
					15	ps_{RMS}
		f > 5kHz (jitter is assumed deterministic, caused by power-supply noise and buffer jitter)			20	ps_{p-p}

Parallel Fiber Module Requirements

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Impedance	R_{IN}		80	100	120	Ω
Transmitter Input Sensitivity					300	mVp-p
Total Jitter Generation		Deterministic and random jitter, peak-to-peak, ($DJ + 16.4 \times RJ_{RMS}$)			80	ps_{p-p}
Receiver Data Output Amplitude		Differential	300		800	mVp-p
Differential Output Impedance	R_{OUT}		80	100	120	Ω
Channel-to-Channel Crosstalk					5	%

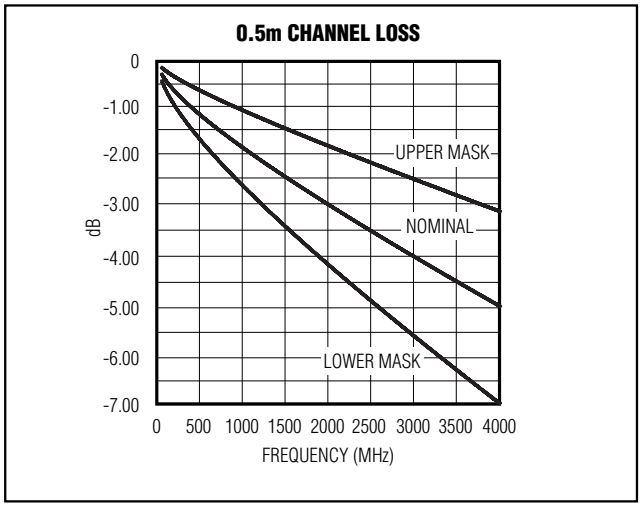


Figure 7. 0.5m Channel Loss Mask

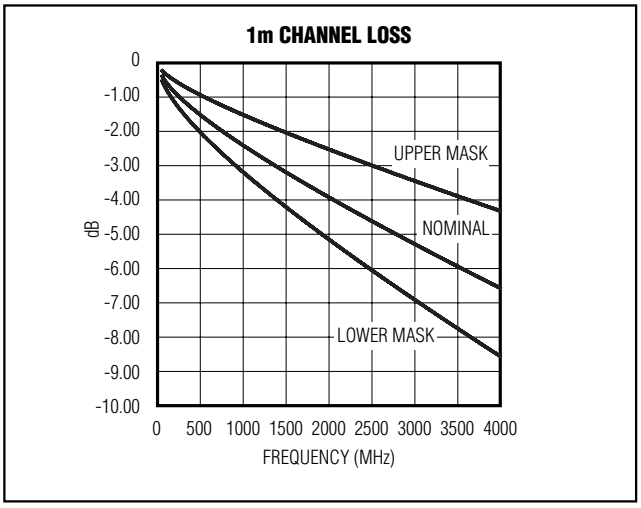


Figure 8. 1.0m Channel Loss Mask

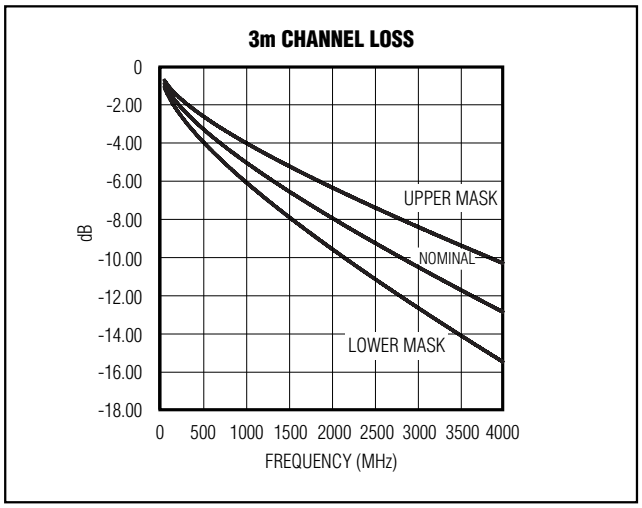


Figure 9. 3.0m Channel Loss Mask

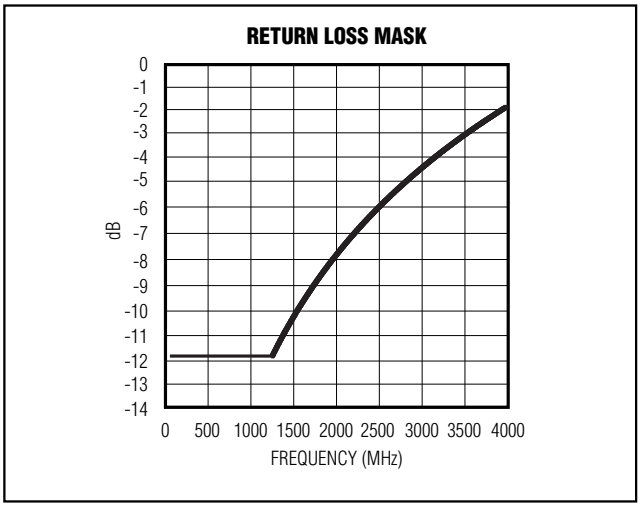
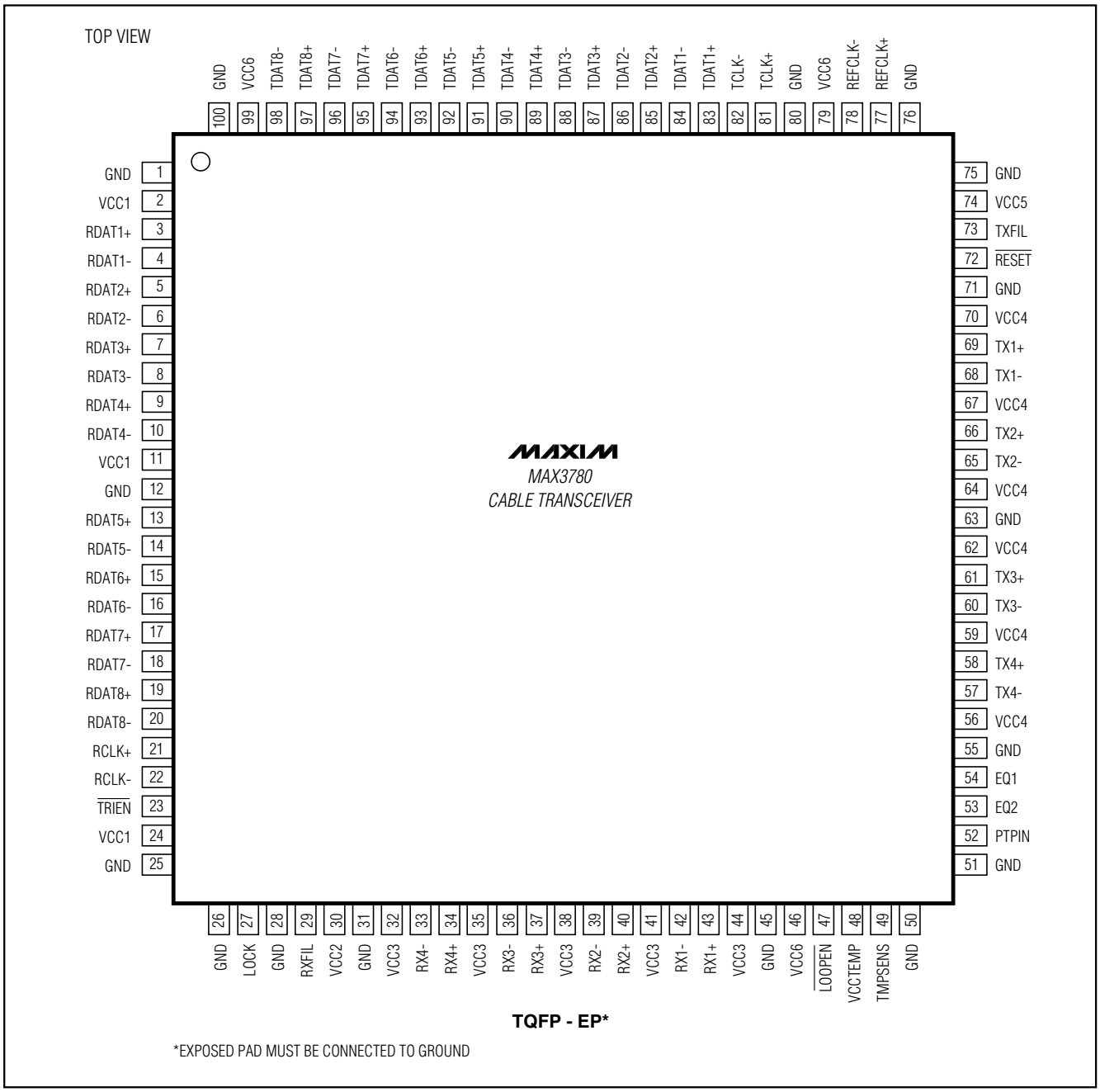


Figure 10. Channel Input Return Loss Mask

Pin Configuration



TQFP - EP*

*EXPOSED PAD MUST BE CONNECTED TO GROUND

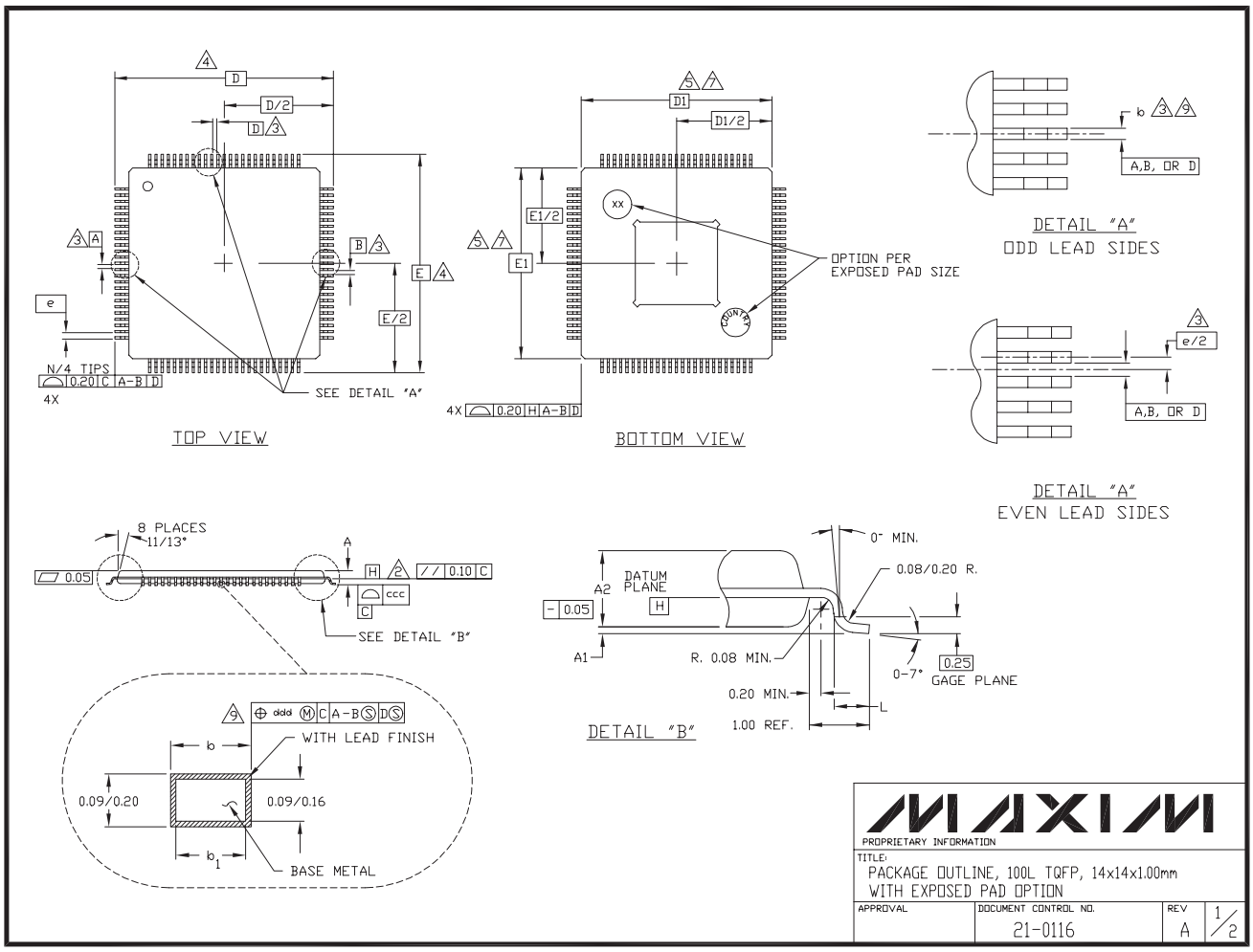
Chip Information

TRANSISTOR COUNT: 15,270

PROCESS: Bipolar

Quad 2.5Gbps Cable Transceiver

Package Information



Package Information (continued)

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M–1994.

2. DATUM PLANE [H] LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.

3. DATUM [A–B] AND [D] TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXITS PLASTIC BODY AT DATUM PLANE [H].

4. TO BE DETERMINED AT SEATING PLANE [C].

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254mm ON D1 AND E1 DIMENSIONS.

6. "N" IS THE TOTAL NUMBER OF TERMINALS.

7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE [H].

8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15mm.

9. DIMENSIONS b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

10. CONTROLLING DIMENSION: MILLIMETER

11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.50mm.

12. THIS OUTLINE IS NOT YET JEDEC REGISTERED.

13. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

14. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 0.05mm.

15. METAL AREA OF EXPOSED DIE PAD SHALL BE WITHIN 0.30mm OF THE NOMINAL DIE PAD SIZE.

16. COUNTRY OF ORIGIN MUST BE MARKED ON THE PACKAGE.

SYMBOL	ALL DIMENSIONS ARE IN MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	—	—	1.20	
A_1	0.05	—	0.15	13
A_2	0.95	1.00	1.05	
D		16.00 BSC.		4
D_1		14.00 BSC.		7,8
E		16.00 BSC.		4
E_1		14.00 BSC.		7,8
L	0.45	0.60	0.75	
N		100		
e		0.50 BSC.		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc	—	—	0.08	
ddd	—	—	0.08	

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 100L TQFP, 14x14x1.00mm WITH EXPOSED PAD OPTION

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0116	A	2/2